Investigation of Class E Amplifier with Nonlinear Capacitance for Any Output $Q$ and Finite DC-Feed Inductance

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SUMMARY This paper investigates the design curves of class E amplifier with nonlinear capacitance for any output $Q$ and finite dc-feed inductance. The important results are; 1) the capacitance nonlinearity strongly affects the design parameters for low $Q$, 2) the value of dc-feed inductance is hardly affected by the capacitance nonlinearity, and 3) the input voltage is an important parameter to design class E amplifier with nonlinear capacitance. By carrying out PSpice simulations, we show that the simulated results agree with the desired ones quantitatively. It is expected that the design curves in this paper are useful guidelines for the design of class E amplifier with nonlinear capacitance.

key words: class E amplifier, nonlinear capacitance on MOSFET, quality factor, DC-feed inductance, SPICE simulations

1. Introduction

Class E switching-mode tuned power amplifiers [1]–[16] have become increasingly valuable building blocks in many applications, e.g., radio transmitters and switching-mode dc power supplies. Because of class E switching, namely, both zero voltage and zero slope of voltage switching, the efficiency of energy conversion is very high at high frequencies. Therefore, a high density of power processing can be achieved, reducing the size and weight of the equipment.

Generally, shunt capacitance $C_S$ is realized by sum of external capacitance and parasitic capacitance on MOSFET. The external capacitance is much larger than the parasitic capacitance under hundred kHz or MHz operation. Therefore, the almost analyses of class E amplifier have assumption that the shunt capacitance $C_S$ works as a linear elements [1]–[9]. At high operating frequencies, however, the parasitic capacitance of the switching device is dominant in the shunt capacitance. In the extreme case, the shunt capacitance is entirely formed by the transistor output capacitance. Since the nonlinear shunt capacitance changes with the drain-to-source voltage, it is difficult to choose a suitable switching device for the class E amplifier. In fact, a switching device that has a nonlinear shunt capacitance generates higher switch peak voltage than the one designed with a linear shunt capacitance. In case the designer uses a lower dc input voltage $V_D$ to avoid breakdown of the switching device, class E switching will not be achieved and therefore chances of switching device being destroyed by heating due to a switching loss.

From the background above, many researchers recently paid attentions to the design of class E amplifier with nonlinear capacitance [10]–[16]. In these researches, the concept of derivations of equivalent linear capacitance allows the design of class E amplifier with nonlinear capacitance. For the derivations of equivalent linear capacitance, however, there are assumptions that are high dc-feed inductance, high loaded quality factor $Q$, 50% duty ratio, and zero active device on resistance since these assumptions simplify the analysis of class E amplifier. Therefore, the guidelines of the design in [10]–[16] are valid for the particular specifications. The important parameters to design class E amplifiers are output $Q$ [2]–[5] and dc-feed inductance [4]–[6]. For miniaturization of class E amplifier, the designers require small dc-feed inductance and low output $Q$. Moreover, low $Q$ is effective to realize class E amplifier with high output power. Since there is no design curve for any output $Q$ and any dc-feed inductance, the designers have no image for adjusting the design values. Therefore, they require strongly the design curves for class E amplifier with nonlinear capacitance for any conditions.

This paper investigates the design curves of class E amplifier with nonlinear capacitance for any output $Q$ and finite dc-feed inductance. By using the design procedure in [9], the design curves can be derived numerically. The important results are; 1) the capacitance nonlinearity strongly affects the design parameters for low $Q$, 2) the value of dc-feed inductance is hardly affected by the capacitance nonlinearity, and 3) the input voltage is an important parameter to design class E amplifier with nonlinear capacitance. By carrying out PSpice simulations, we show that the simulated results agree with the desired ones quantitatively, which guarantees the validity of the design curves in this paper. It is expected that the design curves in this paper are useful guidelines for the design of class E amplifier with nonlinear capacitance.

2. Circuit Description

2.1 Principle Operation

Figure 1(a) shows a circuit topology of class E amplifier. Class E amplifier is composed of a direct voltage source $V_D$, a dc-feed inductor $L_C$, a MOSFET as a switching device $S$,
an external shunt capacitance $C_s$, a series resonant circuit $L_0 - C_0$, and a load resistance $R$. Figures 2 and 3 depict example waveforms of class E amplifiers. The MOSFET is driven by a driving signal $D_r$. While the MOSFET is off, the current through the shunt capacitor produces the voltage $v_s$ across the switch. While the MOSFET is on, on the other hand, it flows through the switch. Since the switching losses are reduced to zero by the operating requirements of zero and zero slope of switch voltage ($v_s = 0$ and $dv_s/dt = 0$) at the turn on transition, called class E switching conditions, the theoretical efficiency of class E amplifier is 100%.

The waveforms of input current $i_C$ and output current $i$ are important in order to design of class E amplifier. The waveforms of $i_C$ and $i$ are affected by the magnitude of dc-feed inductance and loaded quality factor $Q$, respectively.

### 2.2 The Effects of Loaded Quality Factor and DC-Feed Inductance

Figure 2 shows example waveforms of class E amplifier with high dc-feed inductance. If dc-feed inductance $L_C$ is assumed as RF choke, namely high $L_C$, the input current $i_C$ is approximately constant, which is equal to its dc component as shown in Fig. 2. This means that the waveforms are independent of $L_C$ for high $L_C$ since the input current is constant. On the other hand, finite dc-feed inductance, namely, low $L_C$ generates non-constant input current $i_C$ as shown in Fig. 3. The waveforms of $i_C$ varies by changing $L_C$ when $L_C$ is low. Therefore, we cannot assume a particular waveform of the input current for finite dc-feed inductance.

If a loaded quality factor $Q$ is high ($Q > 5$), output current $i$ through the $LC$ resonant circuit is approximately sine wave as shown in Fig. 2. Therefore, sinusoidal output can be assumed for high $Q$. Figure 3 shows the example waveforms of class E amplifier with low output $Q$. In this case, low output $Q$ makes the output current $i$ be non-sinusoidal since high frequency components are passed through $LC$ resonant circuit. The waveforms of $i$ varies by changing out put $Q$ in the range of low $Q$. Therefore, we also cannot assume a
particular waveform of the output current for low output $Q$.

The assumptions of high dc-feed inductance or high output $Q$ are convenient to analysis class E amplifiers. This is because that the dimensions of circuit equations are degenerated by the constant input current $i_{sc}$ and the sinusoidal output current $i$. In the previous papers, class E amplifiers with nonlinear capacitance were analyzed under both assumptions. For high power applications, however, the low output $Q$ is required since the voltage on $LC$ resonant circuit can be suppressed. On the other hand, in case that the designers require the small circuit scale, $L_C$ and $L_D$ should be low. In this case, both low output $Q$ and finite dc-feed inductance are specified for the design.

3. The Nonlinearity of Shunt Capacitance

Generally, shunt capacitance $C_S$ is realized by sum of external capacitance and parasitic capacitance on MOSFET. The problem is that the parasitic capacitance is nonlinear, but the external capacitance is linear [16]. The external capacitance is much higher than the parasitic capacitance under hundred kHz or MHz operation. Therefore, the almost analyses of class E amplifier have assumptions that the shunt capacitance $C_S$ works as a linear elements. These analyses, however, clarify the shunt capacitance $C_S$ is lower and lower as the operating frequency becomes high. Therefore, the parasitic capacitance on MOSFET is dominant under high frequency operations so the designers cannot eliminate it.

From above reason, many researchers recently paid attention to the design of class E amplifier with nonlinear capacitance [10]–[15].

In this paper, we have the following assumptions about the MOSFET.

(i) The shunt capacitance consists of only the parasitic capacitance on the MOSFET like [10]–[15].

(ii) The switching time of MOSFET is enough small to be neglected.

(iii) The MOSFET has infinite off resistance and on resistance $r_S$.

From above assumptions, the MOSFET is expressed as a switch $S$, a switch on resistance $r_S$, and a nonlinear parasitic capacitance between the drain and source $C_{ds}$ as shown in Fig. 1(b). Since the power MOSFET contains a p-n junction body diode, the parasitic capacitance $C_{ds}$ can be expressed by

$$C_{ds} = \frac{C_{j}}{1 + \frac{V_{bi}}{V_{j}}},$$

where $V_{bi}$ is the built-in potential which typically ranges from 0.5 to 0.9 V, $V_S$ is the drain-to-source voltage, $C_{j}$ is the capacitance at $V_S = 0$, and $m$ is the grading coefficient of the diode junction. Figure 4 shows the ratio of $C_{ds}$ to $C_{j}$ as a function of $V_S$ for $V_{bi} = 0.7$ V. From this figure, the parasitic capacitance on MOSFET decreases with the increase of switching voltage $V_S$.

In order to account for the nonlinear capacitance on MOSFET in the class E amplifier, several approaches have been published [10]–[15]. The main approach is the derivations of the equivalent linear capacitance defined as the one that placed in lieu of the nonlinear one. By using the equivalent linear capacitance, it is possible to design class E amplifier with nonlinear capacitance. In [14], the equivalent linear capacitance $C_{equ}$ for $m = 0.5$ is given as

$$C_{equ} = \frac{24 V_{bi} C_{j} b}{(12 V_{bi} + 6 V_{bi} (24 V_{bi} - 24 \pi^2 V_D + \pi^4 V_D) + 9 \pi^2 (V_D)^2 \sqrt{V_{bi} V_D})^{1/2}}.$$  

From this equation, we can find $C_1$ is a function of $V_D$.

The equivalent linear capacitance is, however, derived from the assumptions with a constant input current and sinusoidal output voltage, namely high output $Q$ and RF choke. All design guidelines for class E amplifier with nonlinear capacitance published until now are valid only under the conditions with high output $Q$ and high dc-feed inductance. As mentioned in previous section, the designers require the design of class E amplifier for any conditions including low output $Q$ and low dc-feed inductance. Therefore, we recognize that it is quite important to derive and investigate of design curves of class E amplifier with nonlinear capacitance for various conditions. It is expected the design curves are the important guidelines to design of it.

4. Derivation of Design Curves

In case of the design of class E amplifier with nonlinear capacitance for any output $Q$ and finite dc-feed inductance, the diminutions of circuit equations cannot be degenerated because of non-constant input current and non-sinusoidal output voltage. Therefore, we cannot use the design techniques of the equivalent linear capacitance presented in [10]–[15].

In this paper, the design procedure in [9] is applied to the design of class E amplifier with nonlinear capacitance. This design procedure is the following features.
a. It is unnecessarily to derive the waveform equations in the design procedure. Moreover, the steps of the design except the derivation of circuit equations are carried out with aid of computer.
b. When the circuit equations are derived, class E amplifier can be designed with few efforts. This means that the design procedure can deal with the class E amplifier with the nonlinear parasitic capacitance on MOSFET.
c. The designers prepare only circuit equations and design specifications in the design. There are few limitations for the range of parameters. Namely, it is possible to design class E amplifier with low Q, finite dc-feed inductance, and so on in spite of existence of nonlinear capacitance.

From above reasons, we apply the design procedure in [9] to derive the design curves of class E amplifier with nonlinear capacitance.

4.1 Parameters

At first, the following parameters are defined.

1. \( \omega = 2\pi f \): The operating (switching) angular frequency.
2. \( \omega_0 = 2\pi f_0 = 1/\sqrt{L_0C_0} \): The resonant angular frequency.
3. \( A = f_0/f = \omega_0/\omega \): The ratio of the resonant frequency to the operating frequency.
4. \( B = C_0/C_{\phi} \): The ratio of a resonant capacitance to parasitic capacitance on MOSFET for \( v_S = 0 \).
5. \( H = L_0/L_C \): The ratio of resonant inductance to a dc-feed inductance.
6. \( Q = \omega L_0/R \): The loaded quality factor.
7. \( D \): The switch on duty ratio of the switch S.

In this paper, the parameters \( A \) and \( B \) are important. The parameter \( A \) is very sensitive to the waveforms of class E amplifier. If \( A \) is changed slightly, the performance of class E amplifier entirely varies. This characteristic is applied to the frequency control of class E amplifier [1]. On the other hand, the parameter \( B \) is insensitive to those, especially, output current.

4.2 Circuit Equations

We consider the circuit operation in the interval \( 0 \leq \theta < 2\pi \), where \( \theta \equiv \omega t \) represents angular displacement. The circuit equations are expressed as follows:

\[
\begin{align*}
\frac{dV}{d\theta} &= \frac{H}{QR}(V_D - v_S) \\
\frac{dv_S}{d\theta} &= A^2 B Q R (1 + v_S/V_{bi})^{m}(i_C - v_S/R_S - i) \\
\frac{dC}{d\theta} &= \frac{1}{QR}(v_S - v - Ri) \\
\frac{dv}{d\theta} &= A^2 Q R i.
\end{align*}
\]

In Eq. (3), \( R_S \) means the resistance of the switch S. When we define that the switch S turns on at \( \theta = 0 \), \( R_S \) are given as follows from Assumption of the MOSFET (iii).

\[
R_S = \begin{cases} 
  r_S & \text{for } 0 \leq \theta < 2\pi D \\
  \infty & \text{for } 2\pi D \leq \theta < 2\pi
\end{cases}
\]

In Eqs. (3) and (4), \( H, Q, R, V_D, V_{bi}, m, r_S \) and \( D \) are given as a design specifications. Under the specifications, \( A \) and \( B \) are determined for achieving class E switching conditions, namely,

\[
\begin{align*}
  v_S(2\pi) &= 0 \\
  \frac{dV_S(\theta)}{d\theta} \bigg|_{\theta=2\pi} &= 0.
\end{align*}
\]

The procedure for the derivations of \( A \) and \( B \) is shown in Appendix. By using this design procedure, it is possible to derive the design curves of class E amplifier with nonlinear capacitance on MOSFET for any output \( Q \) and finite dc-feed inductance.

5. Discussion of Results

In this section, we denote and investigate the design curves of class E amplifier with nonlinear capacitance. In first, the design specifications are given as follows: \( R = 1 \Omega, r_S = 0.01 \Omega \) and \( D = 0.5 \). In this paper, we investigate the design curves with any \( Q, H \) and \( V_D \) for \( m = 0 \) and 0.5. The \( m = 0 \) means that the shunt capacitance \( C_{ds} \) works as a linear element. On the other hand, the design curves for \( m = 0.5 \) are shown as a nonlinear element. In this paper we investigate the design curves only for \( m = 0.5 \) as nonlinear shunt capacitance following the previous papers [10], [14] and [16]. By using this design procedure, however, it is easy to derive the design curves for other values of \( m \).

Figure 5 shows the design parameters \( A \) and \( B \) as a function of \( Q \) for \( V_D = 1 \) V and \( H = 0.001 \). This figure shows that the design curves of \( A \) and \( B \) vary rapidly at about \( Q = 5 \). That is because the bailiwick of \( Q = 5 \) is the boundary between under-damped case and over-damped case of the amplifier. For high output \( Q, A \) and \( B \) are almost constant since output voltage \( v_S \) does not change for the variations of \( Q \). On the other hand, the parameters \( A \) and \( B \) vary in the range of low output \( Q \). From this result, we can find that the design values are greatly influenced by the waveforms of the current through the resonant circuit regardless of \( m \). The differences of the design parameters appear between \( m = 0 \) and 0.5. We find the difference of \( A \) for high output \( Q \) is very small. Here, we consider the case that class E amplifier is designed by the procedure for linear shunt capacitance. If shunt capacitance of class E amplifier works as nonlinear element, its equivalent linear capacitance is nearly equals to the designed value of linear shunt capacitance. In high \( Q \) region, Eq. (2) can be applied to consider the equivalent linear capacitance. For the specifications of Fig. 5, the relation is given as \( C_{eq} = 0.6211 C_{\phi} \). By considering this relation and ratio of \( B \) for \( m = 0 \) to one for 0.5, it can be said that the difference of \( B \) is also small for high \( Q \).
These results agree with the claim in [10], that is, the output voltage are not affected by the capacitance nonlinearity. The differences of the design curves are, however, large for low output $Q$. We should note that the claim in [10] is based on the assumption of high output $Q$. The result in this paper denotes that it is quite important to consider a capacitance nonlinearity for low output $Q$, which is a new and important discovery. In this design specification, the minimum values of $Q$ to achieve class E switching conditions are 1.79 and 1.99 for $m = 0$, and 0.5, respectively. The minimum values of $Q$ for nonlinear capacitance are higher than those for linear capacitance.

Figure 6 shows the design parameters $A$ and $B$ as a function of $H$ for $V_D = 1$ V. Here, small $H$ means that the dc-feed inductance $L_C$ is high. For $H < 0.1$, the design curves of $A$ and $B$ are almost constant. In this range, the input current is constant because of the RF choke. On the other hand, the design curves vary in the region of high $H$. This is because that the input current $i_C$ includes ac component and the waveform of it varies by the change of $H$. In Fig. 6, the differences of the design parameters between $m = 0$ and 0.5 become small as $H$ increases. Moreover, the design curves with nonlinear capacitance are close to that with linear capacitance for $Q = 10$. From these results, it is found that the capacitance nonlinearity hardly affects the design of class E amplifier. This claim agrees with one in [10], that is, the input current is not affected by the capacitance nonlinearity. The claim in [10] is valid only the conditions with high dc-feed inductance. We would like to emphasize that the result in this paper is based on the conditions with any dc-feed inductance. We think that the differences of the design curves for $Q = 3$ occurs because of low output $Q$. In this design specification, there are limitations of $H$ for $Q = 3$. They are 5.64 and 5.11 for $m = 0$ and 0.5, respectively.

Figure 7 shows the design parameters $A$ and $B$ as a function of $V_D$ for $H = 0.001$. The design parameters are constant for $m = 0$. It is well known that $V_D$ affects only the amplitude of currents and voltages in case of linear capacitance [7]. From Fig. 7, the differences of the design parameters grow as the input voltage $V_D$ increases. This result is explained as follows by using Fig. 4. For small $V_D$, the switch voltage $v_{S_k}$ is also small. Therefore, the variation of $C_{ds}$ is narrow and the design parameters with nonlinear ca-
The design parameters $A$ and $B$ as a function of $V_D$ for $H=0.001$. (a) Design curve of $A$. (b) Design curve of $B$.

From above results, we can conclude that it is important to consider of capacitance nonlinearity, especially, when the design specification includes low output $Q$ or large $V_D$. If a small circuit scale is required, the design with finite dc-feed inductance is effective for avoiding the affects of the nonlinearity. The designers should note the nonlinearity for high power applications whose specifications include both low output $Q$ and large $V_D$.

### 6. Simulation Verification

In this section, we show the simulation results in order to denote the validity of design curves. In this paper, three simulation results are shown. Two of them are under the same design specifications in the previous section in order to show the validity of Figs. 5–7. The design specifications are given as follows: $f = 5.0$ MHz, $V_D = 1$ V, $R = 1$ $\Omega$, $r_S = 0.01$ $\Omega$, $D = 0.5$, $V_{bi} = 0.7$ $V$ and $m = 0.5$, where $r_S = 0.01$ $\Omega$ is chosen in the meaning of a few percent of $R$. We use a power MOSFET SPICE model Level 3. Table 1 shows the specifications of MOSFET in our simulations which is determined according to those in [14].

At first, $Q=10$ and $H = 0.001$ are given to design the class E amplifier for high output $Q$ and large dc-feed inductance. From these specifications, the design parameters are given as $A = 0.933$ and $B = 0.356$. From $A$ and $B$, the design values are determined as shown in Table 2(a). We confirm these design values are quite similar to those obtained from the design procedure in [14]. From this fact, we can confirm that the design procedure in [9] can apply to the design of class E amplifier with nonlinear capacitance. Figure 8 shows the waveforms by PSpice simulation. In this figure, we find that the input current $i_C$ is constant and the output voltage $v_o$ is sinusoidal because of high output $Q$ and large dc-feed inductance. Moreover, we can confirm that switch voltage $v_S$ is satisfied with class E switching conditions. Next, we design class E amplifier for $Q=3$ and $H = 0.5$, that mean low $Q$ and small dc-feed inductance. Under these specifications, the design parameters are obtained as $A = 0.783$ and $B = 1.034$. From these parameters, the design values are derived as shown in Table 2(b).

<table>
<thead>
<tr>
<th>$D$</th>
<th>0.5</th>
<th>0.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_c$</td>
<td>3183 $\mu$H</td>
<td>919.0 $\mu$H</td>
</tr>
<tr>
<td>$L_b$</td>
<td>318.3 $\mu$H</td>
<td>95.49 $\mu$H</td>
</tr>
<tr>
<td>$C_j$</td>
<td>10.23 $\mu$F</td>
<td>16.71 $\mu$F</td>
</tr>
<tr>
<td>$C_o$</td>
<td>3.65 $\mu$F</td>
<td>17.29 $\mu$F</td>
</tr>
<tr>
<td>$R$</td>
<td>1.02 $\Omega$</td>
<td>1.02 $\Omega$</td>
</tr>
<tr>
<td>$f$</td>
<td>5.0 MHz</td>
<td>5.0 MHz</td>
</tr>
<tr>
<td>$V_D$</td>
<td>1.0 $V$</td>
<td>1.0 $V$</td>
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</table>

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Figures 2 and 3 depict the waveforms from the circuit equation (3) by using Runge-Kutta method. The parameters of Figs. 2 and 3 are identical to those of Figs. 8 and 9, respec-
Fig. 8  Simulation results by PSpice for $Q = 10$ and $H = 0.001$.

Fig. 9  Simulation results by PSpice for $Q = 3$ and $H = 0.5$.

tively. From Figs. 2, 3, 8 and 9, we find that the predicted waveforms from the circuit equations are similar to those by PSpice simulations quantitatively. From these results, it can be said that Figs. 5–7 have a validity to use as guidelines for the design of class E amplifier with nonlinear capacitance.

Finally, the design specifications which are suitable for practical use are given. The design specifications are

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Finally, the design specifications which are suitable for practical use are given. The design specifications are

<table>
<thead>
<tr>
<th>Table 3</th>
<th>Specifications of MOSFET in PSpice simulation for Fig. 10.</th>
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<tr>
<td>$T_{ox}$</td>
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<tr>
<td>$V_{to}$</td>
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<tr>
<td>$C_{gd}$</td>
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</tr>
<tr>
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<tr>
<td>$V_{dd}$</td>
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<table>
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<th>Table 4</th>
<th>Design values of each element for Fig. 10.</th>
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<td>663.3 $\mu$H</td>
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<td>663 nH</td>
</tr>
<tr>
<td>$C_{d}$</td>
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</tr>
<tr>
<td>$C_{o}$</td>
<td>49.0 pF</td>
</tr>
<tr>
<td>$R$</td>
<td>12.5 $\Omega$</td>
</tr>
<tr>
<td>$f$</td>
<td>30.0 MHz</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>40 V</td>
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</tbody>
</table>

Fig. 10  Simulation results by PSpice for $f = 30.0$ MHz, $V_{dd} = 40$ V, $R = 12.5$ $\Omega$, $Q = 10$, and $H = 0.001$. (a) Waveforms by Pspice simulation. (b) Waveforms by numerical prediction.

It is found that $V_{G}$ in Figs. 10(a) and (b) are satisfied with class E switching conditions and waveforms by Pspice simulation are similar to those by numerical predictions quantitatively. We consider slight differences between Figs. 10(a) and (b) are caused by the difference of MOSFET model between Pspice and circuit equation (3). From this result, it can be confirmed that the design procedure introduced in Sect. 4 gives accurate design values under the specifications for practical use which are different from those for the de-
sign curves.

7. Conclusion

This paper has investigated the design curves of class E amplifier with nonlinear capacitance for any output $Q$ and finite dc-feed inductance. By using the design procedure in [9], the design curves can be derived numerically. The important results are; 1) the capacitance nonlinearity strongly affects the design parameters for low $Q$, 2) the value of dc-feed inductance is hardly affected by the capacitance nonlinearity, and 3) the input voltage is an important parameter to design class E amplifier with nonlinear capacitance. By carrying out PSpice simulations, we show that the simulated results agree with the desired ones quantitatively, which guarantees the validity of the design curves in this paper.

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References


Appendix

Determinations of $A$ and $B$

At first, we define $x \in \mathbb{R}^6$ and $\lambda \in \mathbb{R}^6$ as $x(\theta) = [i_4(\theta), v_5(\theta), i_6(\theta), v(\theta)]^T$ and $\lambda = [A, B, D, H, Q, R, V_D, V_{bi}, m, r_s]^T$. From the assumption of the solution $x(\theta) = \phi(\theta, x_0, \lambda) = [\phi_1, \phi_2, \phi_3, \phi_4]^T$ with period $2\pi$, the Poincaré mapping $T(x_0, \lambda)$ is expressed as

$$T(x_0, \lambda) = \phi(2\pi, x_0, \lambda). \quad (A\cdot 1)$$

Therefore, the circuit in the steady state is satisfied with the following transient condition:

$$T(x_0, \lambda) - x_0 = 0 \quad \in \mathbb{R}^6. \quad (A\cdot 2)$$

Moreover, because of class E switching conditions, the equations

$$g_1(2\pi, x_0, \lambda) = \phi_2(2\pi, x_0, \lambda) = 0, \quad (A\cdot 3)$$

$$g_2(2\pi, x_0, \lambda) = \frac{d\phi_2(\theta, x_0, \lambda)}{d\theta} \bigg|_{\theta=2\pi} = A^2 B Q R (\phi_1(2\pi, x_0, \lambda) - \phi_3(2\pi, x_0, \lambda)) = 0, \quad (A\cdot 4)$$

are given. Therefore, we derive the algebraic equations from Eqs. (A-2)–(A-4) as follows,

$$F(x_0, \lambda) = \left[ T(x_0, \lambda) - x_0 \right]$$

$$= \begin{bmatrix}
\phi_1(2\pi, x_0, \lambda) - i_4(0) \\
\phi_2(2\pi, x_0, \lambda) - v_5(0) \\
\phi_3(2\pi, x_0, \lambda) - i_6(0) \\
\phi_4(2\pi, x_0, \lambda) - v(0) \\
\phi_5(2\pi, x_0, \lambda) \\
\phi_6(2\pi, x_0, \lambda)
\end{bmatrix} \quad (A\cdot 5)$$

$$= 0, \quad \in \mathbb{R}^6.$$
In Eq. (A-5), we have 6 algebraic equations and 6 unknown values, namely, \( \dot{i_c}(0), v_C(0), i_L(0), v(0) \), and \( A \) and \( B \): 
\[
\mathbf{u} = [\dot{i_c}(0), v_C(0), i_L(0), v(0), A, B]^T
\]
since the parameters except \( A \) and \( B \) are given as a design specification. As a result, the design of class E amplifier boils down to the derivation of the solution \( \mathbf{u} \).

We solve Eq. (A-5) by using Newton’s method. Newton’s method means that the computations

\[
\mathbf{u}^{k+1} = \mathbf{u}^k - \frac{F(\mathbf{u}^k)}{F'(\mathbf{u}^k)}
\]  

(A-6)

are iterated for \( \|\mathbf{u}^{k+1} - \mathbf{u}^k\| < \delta \) in order to find the unknown values, where \( F' \in \mathbb{R}^{6 \times 6} \) means Jacobian matrix of \( F \), \( k \) is an iteration number and \( \delta \ll 1 \), i.e., \( \delta = 10^{-9} \) in this paper. Then \( \mathbf{u}^{k+1} \) is a solution of (A-5), namely, the design parameters \( A \) and \( B \) can be determined.

In this design procedure, the steps of the design except derivation of the circuit equations are carried out with aid of computer. This means that design values for any parameters can be derived. In this paper, only design curves for \( m = 0 \) and 0.5 are shown. By using this design procedure, it is easy to derive the design curves for other values of \( m \). Similarly, the designers need few efforts to derive the design values for any design specifications that include output \( Q \), finite dc-feed inductance \( L_C \), dc voltage \( V_D \), output resistance \( R \), duty ratio \( D \) and so on.

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