Design of Class DE Inverter with Band-pass Filter

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Abstract—This paper presents design procedure and experimental results class DE inverter with band-pass filter. In the proposed inverter, band-pass filter is used instead of resonant filter in the class DE inverter presented at the previous papers. By using band-pass filter, the sensitivity of output voltage to the operating frequency can be suppressed. By carrying out circuit experiments, we show that the experimental results agree with numerical ones quantitatively. The laboratory experiments achieve 90.4% power conversion efficiency under 2.2W output power and 1 MHz operation.

I. INTRODUCTION

Class DE inverter[1]–[6] achieves high power conversion efficiency under a high frequency operation because of class E switching [7]. Class E switching means that both the switching voltage and the slope of switching voltage are zero when each switch turns on. It is expected that class DE inverter is useful in applications such as AM and PWM transmitters for medical applications, electronic ballasts and so on because of high efficiency and high frequency operation. Class DE inverter presented in the previous papers includes a resonant circuit to acquire sinusoidal output. The output voltage is quite sensitive to the variations of operating frequency. Moreover, class E switching conditions are strict, so not only the class E switching conditions but also zero voltage switching (ZVS) cannot be achieved against the variations of operating frequency [6]. The high sensitivities of output power and switching conditions to the operating frequency are problems for class DE inverter.

The resonant filter is designed to achieve class E switching conditions at a specified the operating frequency. The output characteristic of the resonant filter varies rapidly around a specified operating frequency by changing the operating frequency. It is recognized that the sensitivities are caused by the characteristics of resonant filter. The filter of class DE inverter works to acquire pure sinusoidal output. Therefore, it is allowed that the other types of filter which cut higher harmonics and direct component is applied to class DE inverter.

This paper presents design procedure and experimental results of class DE inverter with band-pass filter. In the proposed inverter, band-pass filter is used instead of resonant filter in the class DE amplifier presented at the previous papers. By using band-pass filter, the sensitivity of output voltage to the operating frequency can be suppressed. Since the proposed circuit is satisfied with class E switching conditions, it achieve high power conversion efficiency under high frequency operation. By carrying out circuit experiments, we show that the experimental results agree with numerical ones quantitatively. The laboratory experiments achieve 90.4% power conversion efficiency under 2.2W output power and 1 MHz operation. Moreover, it is confirmed that the proposed inverter achieves ZVS operation for the lower frequency than the nominal frequency, which also an important result in this paper.
II. Circuit Description

A. Class DE inverter

Figure 1 shows a circuit topology of a Class DE inverter. Class DE inverter is composed of an input voltage $V_{cc}$, two switches $S_1$ and $S_2$ with anti-parallel diode $D_{S1}$ and $D_{S2}$, shunt capacitors $C_{S1}$ and $C_{S2}$, a resonant filter $L_0 - C_0$ and load resistance $R$. The example waveforms of class DE inverter are shown in Fig. 2 when the switch on duty ratio of each switch is 0.25. The switch on duty ratio of class DE inverter can be specified to any values from zero to 0.5. This is because both of switches are on state simultaneously for more than 0.5 of the switch on duty ratio, which causes short circuit in the inverter and makes the circuit broken. The switches are driven by a driving pattern of $D_{r1}$ and $D_{r2}$ in Fig. 2, where $D_{r1}$ and $D_{r2}$ drive $S_1$ and $S_2$, respectively. The driving pattern generates a dead time that the period when one switch has tuned off before the other switch has turned on. During the dead time, the output current $i_0$ charges one shunt capacitor and discharges the other shunt capacitor, and the midpoint voltage between two switches, namely, $v_{S1}$ becomes $V_{cc}$ or zero at the end of the dead time, allowing class E switching conditions. As shown in Fig. 2, the maximum voltages across the switches are equals to the input voltage $V_{cc}$. This is an advantage of class D type of inverter compared with class E inverter. Class DE inverter has the both advantages of class D inverter and class E inverter, namely, high power conversion efficiency under high-frequency operation because of class E switching and low switch-voltage stress. Class DE inverter achieves high power conversion efficiency under a high operation frequency (MHz order) because of class E switching conditions [7]. Class E switching conditions that both the switching voltage and the slope of switching voltage are zero when each switch turns on.

B. Sensitivity of Output Power and Switching Conditions to Operating Frequency

The output voltage is quite sensitive to the variations of operating frequency. Moreover, not only class E switching conditions but also zero voltage switching (ZVS) cannot be achieved against the variations of operating frequency since class E switching conditions are strict [6]. The high sensitivities of output power and switching conditions to the operating frequency are problems for class DE inverter. In the previous papers [1]-[6], class DE inverter uses the resonant filter. This filter is designed to achieve class E switching conditions at 1MHz of the operating frequency. However, the output characteristic varies rapidly around nominal operating frequency, that is, 1MHz of operating frequency as shown in Fig. 4. It is recognized that the sensitivities are caused by the characteristics of resonant filter.

The filter of class DE inverter works to acquire pure sinusoidal output. Therefore, it is allowed that the other type of filter which cut higher harmonics and direct component is applied to class DE inverter. If the output characteristic of the filter as a function of frequency is flat at the nominal operating frequency compared with the resonant filter, it is expected that the sensitivity of output power to the operating frequency is relaxed.

C. Proposed inverter

This paper presents class DE inverter with band-pass filter as shown in Fig. 3. In the proposed inverter, band-pass filter $L_1 - C_1 - L_2 - C_2$ is used as shown in Fig. 3 instead of the resonant filter $L_0 - C_0$ in Fig. 1. The band-pass filter passes frequencies with a certain bandwidth. If we set the bandwidth to cut the higher harmonics and direct component, pure sinusoidal output voltage is derived.

The fundamental operations of the proposed inverter is same as class DE inverter with resonant filter, namely, class E switching is applied to the proposed inverter. Because of class E switching and class D topology, the proposed inverter also achieves high power conversion efficiency under high frequency operation and low switch-voltage stress. Moreover, since the output characteristics as a function of
III. Circuit Design

The proposed circuit has six memory elements as shown in Fig. 3. This means that the proposed circuit expresses high dimensional circuit equations. It is difficult to derive the analytical expressions of the waveform equations of the proposed converter. As a result, it is impossible to derive the element values which satisfy class E switching regardless of dimensions of circuit equations. Therefore, we think that the element values of the proposed inverter are easily given for achieving class E switching by using this design procedure.

A. Assumptions

In order to derive the waveforms of the inverter, we give the following assumptions.

i. The switching devices, namely MOSFETs including anti-parallel diode have zero switching times, large off resistance enough to neglect the current through the switches, and nonzero on resistance. On resistances of the MOSFETs and the anti-parallel diodes are stated as \( r_s \) and \( r_{DS} \), respectively. In this paper, we use a same kind of the MOSFETs for the switches. Therefore, it is assumed that a value of on resistance of one MOSFET is identical that of another MOSFET.

ii. Shunt capacitance of each switching device, namely \( C_{S1} \) and \( C_{S2} \) include switch device capacitance. The equivalent series resistance of each capacitances can be neglected.

iii. In this paper, we use the second order constant K filter as a band-pass filter.

iv. All passive elements including switch on resistors operate as linear elements.

B. Parameters

We define the following parameters of the circuit in order to express circuit equations.

1. \( \omega = 2\pi f \) : The operating angular frequency.
2. \( X = \omega C_S = \omega (C_{S1} + C_{S2}) \)
3. \( \alpha = f_w/f_c \) : The ratio of bandwidth to center frequency of band-pass filter.
4. \( \beta = f_s/f_c \) : The ratio of operating frequency and center frequency of band-pass filter.
5. \( Z \) : The impedance of band-pass filter when band-pass filter is second order constant K filter.
6. \( D = D_{S1} = D_{S2} \) : The switch on duty ratio.

It is inevitable that two switch is same inverter are on state simultaneously for \( D > 0.5 \). This causes short circuit and breaks the inverter. Moreover, the dead time must be needed in order to achieve Class E switching. Therefore, the range of \( D \) is determined as \( 0 < D < 0.5 \).

C. Circuit Equations

Following above assumptions, the equivalent circuit of the proposed inverter is shown in Fig. 3(b). We consider operations at \( 0 \leq \theta < 2\pi \) to design circuit, where \( \theta = \omega t \) presents the angular time. Using the parameters, the circuit equations are expressed as follows:

\[
\begin{align*}
\frac{dv_{S1}}{d\theta} &= -\frac{1}{X} \left( i_2 + \frac{1}{R_{S1}} \right) v_{S1} - \frac{V_D}{R_{S2}} \\
\frac{dv_1}{d\theta} &= -\frac{Z}{\alpha^2} \left( i_2 - i_1 - \frac{v_1}{R} \right) \\
\frac{di_1}{d\theta} &= \frac{1}{Z} \left( v_{S1} - v_2 - v_1 \right)
\end{align*}
\]

In (1), \( R_{S1} \) and \( R_{S2} \) are the equivalent resistance of MOSFETs \( S_1 \) and \( S_2 \), respectively. When the switch voltage is to be negative, the anti-parallel diode including the MOSFET turns on. Therefore, the switch resistances \( R_{S1} \) and \( R_{S2} \) are given as follows.

\[
\begin{align*}
R_{S1} &= \begin{cases} 
R_s & \text{for } 0 \leq \theta \leq 2\pi D_{r_1} \\
\infty & \text{for } 2\pi D_{r_1} \leq \theta \leq 2\pi \text{ and } v_{S1} \geq 0
\end{cases} \\
R_D &= \begin{cases} 
R_s & \text{for } 2\pi D_{r_1} \leq \theta \leq 2\pi \text{ and } v_{S1} < 0
\end{cases}
\end{align*}
\]

\[
R_{S2} &= \begin{cases} 
\infty & \text{for } 0 \leq \theta \leq \pi, \pi + 2\pi D_{r_2} \leq \theta \leq 2\pi \\
r_s & \text{for } \pi \leq \theta \leq \pi + 2\pi D_{r_2} \text{ and } v_{S2} \geq 0 \\
r_D & \text{for } \pi \leq \theta \leq \pi + 2\pi D_{r_2} \text{ and } v_{S2} < 0
\end{cases}
\]

When we define \( x(\theta) = [x_1, x_2, ..., x_5]^T = [v_{S1}, v_1, v_2, i_1, i_2]^T \in \mathbb{R}^5 \), (1) can be written as

\[
\frac{dx}{d\theta} = f(\theta, x, \lambda),
\]

where \( \lambda = [X, \alpha, \beta, Z, f, r_{S1}, r_{S2}, R, V_{cc}, D] \in \mathbb{R}^{10} \).

D. Conditions for the Design

We assume (1) has a solution \( x(\theta) = \varphi(\theta, x_0, \lambda) = [\varphi_1, \varphi_2, ..., \varphi_5]^T \) defined on \( -\infty < \theta < \infty \) with every initial condition \( x_0 \) and every \( \lambda : x(0) = \varphi(0, x_0, \lambda) \).

If the proposed inverter is in the steady state, the equation:

\[
\varphi(\theta + 2\pi, x_0, \lambda) = \varphi(\theta, x_0, \lambda) \quad \forall \theta
\]

is given. Therefore,

\[
\varphi(2\pi, x_0, \lambda) - \varphi(0, x_0, \lambda) = 0 \quad \in \mathbb{R}^5
\]

is given as the boundary conditions between \( \theta = 0 \) and \( \theta = 2\pi \).

In order to design the proposed inverter, we have to consider the conditions for class E switching. The class E frequency is flat compared with resonant filter by using band-pass filter, it is expected that the problems of sensitivities to the operating frequency are improved.

Other operation of the circuit is same as the circuit of Fig. 2.
switching mean that both the voltage and the slope of the voltage of the switch are zero when each switches $S_1$ and $S_2$ turns on. Therefore, the equations

$$\varphi_1(2\pi, x_0, \lambda) = 0, \quad (7)$$

$$\left. \frac{d\varphi_1(\theta, x_0, \lambda)}{d\theta} \right|_{\theta=2\pi} = -\frac{1}{X}(\varphi_5(2\pi, x_0, \lambda) = 0. \quad (8)$$

and,

$$\varphi_1(\pi, x_0, \lambda) = V_{cc}, \quad (9)$$

$$\left. \frac{d\varphi_1(\theta, x_0, \lambda)}{d\theta} \right|_{\theta=\pi} = -\frac{1}{X}(\varphi_5(\pi, x_0, \lambda) = 0. \quad (10)$$

are given. If (7) and (8) are valid, (9) and (10) are also valid simultaneously because of symmetry of the waveform. In these equations, we have 7 algebraic equations and 5 unknown initial values. Therefore, 2 parameters can be set as the design parameters from 10 parameters. In this paper, we set $X$ and $\alpha$ as unknown parameters. And the other parameters are given as the design specifications.

We have to determine design parameter to achieve there 7 equations simultaneously. For the decision of design parameters, some techniques for numerical calculation are applied. Specifically, applying Runge-Kutta method and Newton’s method, the unknown parameters can be found, and the design values, that is, $X$ and $\beta$ are determined. The procedure for calculations of Newton’s method is the same as in [8].

IV. DESIGN CURVE

At first, the design specifications are given as follows: $f = 1.000\text{MHz}$, $V_{cc} = 20\text{V}$, $R = 40\Omega$, $V_0 = 9.5\text{V}$, $D = 0.25$, $r_s = 0.16\Omega$ and $r_D = 1.54\Omega$ are given since IRF 530 MOSFET are used.

Figures 5 and 6 shows the design curves of $X$ and $\beta$, output voltage $V_0$ and power conversion efficiency $\eta$ as a function of the impedance of band-pass filter $Z$ for $\alpha = 0.3, 0.5$ and 0.7.

For the derivations of the curves in Fig. 5, the output voltage $V_0$ and the power conversion efficiency $\eta$ are given as

$$V_0 = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \{v_1(\theta)\}^2 d\theta}. \quad (11)$$

$$\eta = \frac{P_{out}}{P_{in}}. \quad (12)$$

where, $P_{in} = V_{cc}I_{in}$ and $P_{out} = V_0^2/R$ express the input power and output power. For the calculation of $P_{in}$, the input current $I_{in}$ is given as

$$I_{in} = \frac{1}{2\pi} \int_0^{2\pi} \{i_{S_2}(\theta) + i_{C_1}(\theta)\} d\theta \quad (13)$$

$$= \frac{1}{2\pi} \int_0^{2\pi} \frac{v_{S_1}(\theta)}{R_{S_1}(\theta)} - i_2(\theta) \} d\theta. \quad (14)$$

In this paper, we adapted the trapezoidal method to calculate a integral.

From Fig. 5(a), when the impedance of the filter $Z$ is smaller than $2\Omega$, $X$ rapidly decrease as decreasing $Z$. This means that $C_1$ become large with the decrease of $Z$. From Fig. 5(b), it is found that the center frequency $f_c$ is high as the impedance of $Z$ increases. Moreover, $\beta$ increases with the decrease of $\alpha$. This result shows that the wide bandwidth is needed in case that the center frequency of the band-pass filter is high. From Fig. 5(c) denotes that the output voltage increases with the increase of the impedance $Z$. Moreover, the output voltage is independent on a value of $\alpha$. Therefore, $Z = 5.0\Omega$ is given because of a specified output voltage. From Fig. 5(d) shows that the power conversion efficiency becomes high as impedance $Z$ increase, It also becomes high with the increase of $\alpha$. The currents through the switches increase by the decrease of $\alpha$. Therefore, the power losses in on resistance of MOSFETs increase and the power conversion efficiency becomes low. Because of requirement of high power conversion efficiency, $\alpha = 0.7$ is given.

From above consideration, the parameters of the band-pass filter is determined as $Z=5.0\Omega$ and $\alpha =0.7$. Simultaneously, the design parameters are derived as $X=0.05\Omega$ and $\beta =0.890$. Figure 6 shows the output characteristic of the designed band-pass filter as a function of operating frequency $f$. In this case, the center frequency and the bandwidth of the band-pass filter are determined as the center frequency $f_c = 1.12\text{MHz}$ and band-width $f_m = 0.64\text{MHz}$. From this figure, it is confirmed that the output characteristic is flat compared with resonant filter.

V. EXPERIMENTAL RESULTS

In this section, circuit experiments are shown. From the discussion in previous section, the element values are
determined as shown in Tab. 1.

Figure 7 shows the examples of experimental waveforms by changing the operating frequency. Figure 7 (a) shows the numerical and experimental waveforms for \( f = 1.00 \text{MHz} \). From this figure, we can confirm the operation of \( v_{S1} \) achieves class E switching. In this paper, we define the state in Fig. 7 (a) as nominal state. In the nominal state, the proposed inverter achieves 90.4 % power conversion efficiency. Figure 7 (b) shows the waveforms for \( f = 0.95 \text{MHz} \), which is smaller than the nominal operating frequency. From this figure, the waveform of the switch \( S1 \) never achieves class E switching conditions, but is satisfied with ZVS. We want to emphasis ZVS never appears against the frequency variations on class DE inverter with resonant filter [6]. The result of Fig. 7(b) suggests that the proposed circuit is applicable to wider fields compared with class DE inverter with resonant filter by using ZVS region effectively. Figure 7 (c) shows the waveforms for \( f = 1.05 \text{MHz} \) which is larger than the nominal operating frequency. From this figure, when operating frequency increases, neither class E switching nor ZVS are achieved. In this case, large switching losses are generated because of non-ZVS.

Figure 8 shows the characteristics of the output voltages as a function of the frequency. From this figure, we pay attention to the variation of the output voltage when the operating frequency varies ±5% from 1.00MHz. The output voltage of class DE inverter with resonant filter in [6] is changed from 65% to 153% of the nominal output voltage. On the other hand, the output voltage of the proposed inverter varies from 87% to 120% of the nominal output voltage. From this result, we can confirm the sensitivity of the output voltage to the operating frequency suppresses by using band-pass filter instead of resonant filter.

Figure 9 shows the characteristics output voltage and the power conversion efficiency as functions of operating frequency \( f \), input voltage \( V_{cc} \) and load resistance \( R \). The characteristics as a function of operating frequency \( f \) is shown in Fig. 9 (a). From this figure, we can find the output voltage is similar to the characteristc of filters in Fig. 4. Moreover, when the operating frequency decrease from 1MHz, the degradation of power conversion efficiency is suppressed. Because proposed inverter achieves ZVS. Figure 9 (b) shows the characteristics as a function of input voltage \( V_{cc} \). This figure denotes that the output voltage is the proportion to the input voltage. Moreover, the power conversion efficiency is constant regardless of input volt-

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**TABLE I**

<table>
<thead>
<tr>
<th></th>
<th>Calculated (µH)</th>
<th>Measured (µH)</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_1 )</td>
<td>0.496</td>
<td>0.496</td>
<td>0.00%</td>
</tr>
<tr>
<td>( L_2 )</td>
<td>1.013</td>
<td>1.012</td>
<td>0.10%</td>
</tr>
<tr>
<td>( C_{s1} )</td>
<td>4.52</td>
<td>4.50</td>
<td>−0.44%</td>
</tr>
<tr>
<td>( C_{s2} )</td>
<td>4.52</td>
<td>4.51</td>
<td>−0.22%</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>40.51</td>
<td>40.49</td>
<td>−0.05%</td>
</tr>
<tr>
<td>( C_2 )</td>
<td>19.85</td>
<td>19.84</td>
<td>−0.05%</td>
</tr>
<tr>
<td>( R )</td>
<td>40.0</td>
<td>39.9</td>
<td>−0.03%</td>
</tr>
<tr>
<td>( D )</td>
<td>0.25</td>
<td>0.25</td>
<td>0.00%</td>
</tr>
<tr>
<td>( f )</td>
<td>1.00MHz</td>
<td>1.00MHz</td>
<td>0.00%</td>
</tr>
<tr>
<td>( V_{cc} )</td>
<td>20.0</td>
<td>20.0</td>
<td>0.00%</td>
</tr>
<tr>
<td>( r_S )</td>
<td>0.16</td>
<td>0.16</td>
<td>0.00%</td>
</tr>
<tr>
<td>( r_D )</td>
<td>1.54</td>
<td>1.54</td>
<td>0.00%</td>
</tr>
<tr>
<td>( V_o )</td>
<td>9.37</td>
<td>9.24</td>
<td>−1.39%</td>
</tr>
<tr>
<td>( \eta )</td>
<td>92.7%</td>
<td>90.4%</td>
<td>−2.48%</td>
</tr>
</tbody>
</table>
age $V_{cc}$, inverter. Figure 9 (c) shows the characteristics as a function of load resistance $R$. From this figure, when the load resistance is small, the output voltage is the proportion to the load resistance. The increase of the output voltage saturates if the load resistance is large. Moreover, the power conversion efficiency decreases as the load resistance increases. From Figs. 7–9 and Tab. 1, it is confirmed that the experimental results agree with numerical ones quantitatively.

VI. Conclusion

This paper has presented design procedure and experimental results for class DE inverter with band-pass filter. By using band-pass filter, the sensitivity of output voltage to the operating frequency can be suppressed. By carrying out circuit experiments, we show that the experimental results agree with numerical ones quantitatively. The laboratory experiments achieve 90.4% power conversion efficiency under 2.2W output power and 1 MHz operation. Moreover, it is confirmed that the proposed inverter achieves ZVS operation for the lower frequency than the nominal frequency, which also an important result in this paper.

References


Fig. 8. Characteristics of the output voltages as a function of the operating frequency.

Fig. 9. Output voltage and the power conversion efficiency by the variations of several parameters (a) As a function of the operating frequency, (b) As a function of the input voltage, (c) As a function of the load resistance.