Analysis and design of class $E$ power amplifier considering MOSFET parasitic input and output capacitances

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Abstract: In this study, design theory and analysis for the class $E$ power amplifier (PA), considering the metal oxide semiconductor field effect transistor (MOSFET) parasitic input and output capacitances, are proposed. The input resistance and capacitances cause non-ideal input voltage at gate terminal, which affect the specifications of the class $E$ PA. In the proposed study, non-linear drain-to-source, linear gate-to-drain and linear gate-to-source MOSFET parasitic capacitances are considered, while zero voltage and zero derivative switching conditions are achieved. Moreover, the input resistance and the value of the input voltage are taken into account in the design theory. According to the obtained results, the duty cycle of the MOSFET depends on the MOSFET threshold voltage, input voltage, input series resistance, and some other parameters, which will be explained in this study. A design example is finally given to describe the design procedure at 1 MHz operating frequency along with the experimental result. The circuit simulation is also performed using PSpice software. The measured results showed quantitative agreements with simulation and theory results.

1 Introduction

Power amplifier (PA) is a high power consuming block in any communication system. Therefore, high efficiency PAs are important in industrial and communication applications [1–7]. The class $E$ PA is a good solution to achieve high efficiency, compared with the other classes of operation [8–13].

Recently, several analyses have been performed on the class $E$ PA, considering the drain-to-source capacitance as a non-linear or linear shunt capacitance [14–19]. Most of studies were carried out under the assumption of linear shunt capacitance. Recently, non-linear drain-to-source capacitance has become a subject of interest. Several studies show that it is indispensable to consider the non-linearity of drain-to-source capacitance.

The shunt capacitance is necessary to satisfy the class $E$ zero voltage and zero derivative switching (ZVS and ZDS) conditions [20–23]. These conditions are essential for the class $E$ PA to achieve zero switching loss, low noise and high efficiency at high frequencies [24–27]. However, the shunt capacitance is not the only element, affecting the ZVS and ZDS conditions.

Moreover, some approaches suggested that it is important to consider the gate-to-drain capacitance [28–31]. In [10, 19, 29–33], the metal oxide semiconductor field effect transistor (MOSFET) drain-to-source and gate-to-drain parasitic capacitances are taken into account. Some of these approaches have assumed linear MOSFET drain-to-source parasitic capacitance [28–31]. Analysis of class $E$ ZVS PA with MOSFET non-linear drain-to-source parasitic capacitance at any grading coefficient is investigated in [10]. In this research the grading coefficient of the drain-to-source capacitance is assumed as a new degree of freedom in design of class $E$ PA. However, the other parasitic elements, such as input capacitances and gate resistance are not considered.

In [29], a class $E$ PA is physically analysed. However, a straightforward design procedure for the circuit parameters is not proposed. In [30], only the effect of feedback capacitance is investigated on the output current and the output power, while the other specifications of the class $E$ amplifier are not mentioned. The effect of feedback capacitance ($C_{gs}$) is considered in [31], but the switch voltage is approximated for the sake of simplicity. In [32, 33] the gate-to-source ($C_{gd}$) capacitance is also considered, however, the switch voltage equation is not obtained. The effects of the parasitic resistances of class $E$ amplifier are studied in [34], but the input parasitic elements are not considered in this research.

A class-$E$ PA design considering MOSFET non-linear drain-to-source and non-linear gate-to-drain capacitances at any grading coefficient is investigated in [35]. The duty cycle of 0.5 and variable grading coefficients for drain-to-source and gate-to-drain capacitances are considered in the assumptions of this research.

To the best of the authors’ knowledge, effects of the MOSFET gate resistance along with the MOSFET parasitic input and output capacitances have not been considered in any analysis of the class $E$ PA, while the actual MOSFET models include these mentioned parasitic elements. The device parasitic elements can severely impact the performance of the class $E$ PA, at high frequencies [29]. These parameters, however, should be considered, in the practical class $E$ PA design and fabrication to have a more accurate design.

In the proposed analysis, the effects of the MOSFET parasitic input capacitances ($C_{gs}$ and $C_{gd}$) along with the parasitic output capacitance ($C_{ds}$) are investigated. Moreover, the effect of input series resistance ($R_s$) is investigated and the value of input switching voltage is taken into account. This consideration results in more accurate design in class $E$ PA. In power MOSFETs, $C_{gs}$ and $C_{gd}$ depend on the voltages across them because they are affected by depletion layers within the device [36]. However, $C_{ds}$ has only a small voltage change across it, consequently a small capacitance change. Hence, it is considered as a linear capacitance in this paper. The waveforms and the design equations are extracted for achieving the ZVS and ZDS conditions in the class $E$ PA.


2 Analysis and design equations

A typical class E PA structure is shown in Fig. 1a, consisting of a MOSFET as a switch device, DC supply voltage ($V_{DC}$), series resonant RLC filter, shunt capacitance ($C_{sh}$) and a dc-feed inductance ($L_{RFC}$). The shunt capacitance consists of MOSFET parasitic capacitance ($C_{gd}$) and an external capacitance, which only $C_{gd}$ is considered in this manuscript. The resonant inductor is divided into $L_v$ and $L_x$. The $L_v$ with $C$ form an ideal filter to resonant in the operating frequency and the $L_x$ shifts the phase of the output current [28]. The circuit which is used for analysis of the class E PA in the proposed paper is shown in Fig. 1b. $C_{gs}$, $C_{gd}$ and $C_{gdo}$ are specified in the figure, considered for theory analysis. The input series resistance is also shown in this figure ($R_s$), which represents both the MOSFET gate resistance and output resistance of the amplifier driver. The analyses and design equations in this paper are presented under the assumptions, given in Table 1.

The relation between the currents of feedback capacitance ($i_{gfs}$), dc-feed inductance ($L_{dc}$), load ($i_o$) and the non-linear capacitance ($i_{sh}$) can be obtained via a KCL node equation for the $v_s$ node as follows

$$I_{DC} = i_o + i_{gfs} + i_s + i_{sh}. \quad (1)$$

According to the sixth assumption in Table 1, during the first half of the period, the switch is off and $i_s$ is zero. Due to the high value of $Q$, the output current is sinusoidal wave and assumed to be

$$i_s(\theta) = I_w \sin (\theta + \varphi), \quad (2)$$

where, $I_w$ is the output current amplitude, $\theta = \omega t$, and $\varphi$ is the phase shift between source voltage and the output current. The non-linear shunt capacitance can be defined as [14]

$$C_{sh} = \frac{C_{gd}}{1 + v_s/V_{bi}}, \quad (3)$$

where, $v_s$ is the switch voltage, $C_{gd}$ is the drain-to-source capacitance at $v_s = 0$, and $V_{bi}$ is the built-in potential of the MOSFET body diode, which is typically from 0.5 to 0.9 V for silicon transistors. The gate-to-drain and gate-to-source parasitic capacitances are assumed linear and can be obtained as follows

$$C_{gs} = W \times C_{gdo}. \quad (4)$$

and

$$C_{gd} = W \times C_{gdo}. \quad (5)$$

$C_{gdo}$ and $C_{gdo}$ are the gate-to-source and the gate-to-drain capacitances per unit gate width, given in the PSpice model. For obtaining the corresponding gate-to-source and the gate-to-drain parasitic capacitances they should be multiplied by the gate width, $W$, as shown in (4) and (5). According to (2)-(5), (1) can be rewritten as

$$I_{DC} = I_w \sin (\theta + \varphi) + \omega C_{gd} \left( \frac{dv_s}{d\theta} - \frac{dv_{gs}}{d\theta} \right) + \frac{\omega C_{gd}}{\sqrt{1 + v_s/V_{bi}}} \frac{dv_s}{d\theta}. \quad (6)$$

Integration from both sides of (6) gives the following equation

$$\int_0^\theta I_{DC} d\theta = \int_0^\theta I_w \sin (\theta + \varphi) d\theta + \omega C_{gd} \int_0^\theta \frac{dv_s}{d\theta} - \omega C_{gd} \int_0^\theta \frac{dv_{gs}}{d\theta} + \int_0^\theta \frac{\omega C_{gd}}{\sqrt{1 + v_s/V_{bi}}} dv_s, \quad (7)$$

where $\theta_1$ is the angle, in which the gate-to-source voltage has decreased to the threshold voltage of the MOSFET ($\theta_1$th). Another

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**Table 1 Analysis assumptions**

<table>
<thead>
<tr>
<th>Number</th>
<th>Assumptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>duty cycle of the input voltage is 0.5. However, the duty cycle of the MOSFET is not equal to 0.5. It depends on the $v_{gs}$ and threshold voltage of the MOSFET</td>
</tr>
<tr>
<td>2</td>
<td>grading coefficient of MOSFET non-linear output capacitance is constant and equal to 0.5 ($m = 0.5$)</td>
</tr>
<tr>
<td>3</td>
<td>$C_{gs}$ and $C_{gs}$ are linear capacitances, while $C_{gd}$ is a non-linear capacitance</td>
</tr>
<tr>
<td>4</td>
<td>The only shunt capacitance is the MOSFET $C_{gd}$ parasitic capacitance</td>
</tr>
<tr>
<td>5</td>
<td>gate to source voltage is not ideal and the input resistance is considered, as shown in Fig. 1b</td>
</tr>
<tr>
<td>6</td>
<td>input voltage is zero until $0 \leq \theta &lt; \pi$ and equal to $V_s$, at $\pi \leq \theta &lt; 2\pi$</td>
</tr>
<tr>
<td>7</td>
<td>gate to source and switch voltages begin from $v_{gs}(0) = V_s$, and $v_{gs}(0) = 0$ at $\theta = 0$</td>
</tr>
<tr>
<td>8</td>
<td>switch voltage is zero until the gate to source voltage decreases to threshold voltage ($\theta_1$th) at $\theta_1$</td>
</tr>
<tr>
<td>9</td>
<td>on resistance of the MOSFET is zero while the off resistance is infinite. Hence the MOSFET works as an ideal switch</td>
</tr>
<tr>
<td>10</td>
<td>The dc-feed inductance $L_{dc}$ is large enough to ignore the current ripple through it</td>
</tr>
<tr>
<td>11</td>
<td>output current is a pure sine wave at the output frequency, due to large assumption of loaded quality factor ($Q = 10$) of the output resonant</td>
</tr>
<tr>
<td>12</td>
<td>ZVS and ZDS conditions do not lead to best efficiency when parasitic elements are considered; however, these conditions are assumed to solve the equations. The ZVS and ZDS conditions are, respectively, $v_s(\pi) = 0$ and $dv_s(\theta)/d\theta = 0$, at $\theta = \pi$</td>
</tr>
</tbody>
</table>
KCL at $v_{gs}$ node results in
\[
\frac{v_{gs} - v_{in}}{R_s} + \omega C_{gd} \left( \frac{dv_{gs}}{d\theta} - \frac{dv}{d\theta} \right) + \omega C_{gd} \frac{dv_{gs}}{d\theta} = 0, \tag{8}
\]
where $v_{in}$ is the input voltage, which is a square wave and $v_{gs}$ is voltage of the gate-to-source capacitance. The relation between $v_{gs}$ and $v$ could be obtained from (7), which can be written as
\[
v_{gs} = V_{th} + v + 2gV_{bi}\sqrt{1 + v/v_{bi}} - 2gV_{bi}h(\theta). \tag{9}
\]
The initial gate-to-source voltage at $\theta_1$ is equal to $\pi/8$ according to the eighth assumption. The parameters $g$ and $h(\theta)$ are defined as
\[
g = \frac{C_{gd}}{C_{gs}}, \tag{10}
\]
and
\[
h(\theta) = \left[ I_{DC} \times (\theta - \theta_1) + I_n \left[ \cos(\theta + \varphi) - \cos(\theta_1 + \varphi) \right] \right] + 1. \tag{11}
\]
The describing differential equation for the switching voltage can be obtained by substituting (6) and (9) in (8).
\[
\frac{dv}{d\theta} \left( \omega R_s C_{gd} + \frac{g_k}{\sqrt{1 + v/v_{bi}}} \right) = \frac{kI_{DC} - I_n \sin(\theta + \varphi)}{\omega C_{gd}} - v - v_{in} - 2gV_{bi}\sqrt{1 + v/v_{bi}} - h(\theta), \tag{12}
\]
where $k$ is defined as follows
\[
k = \omega R_s \left( C_{gd} + C_{gs} \right). \tag{13}
\]
Equation (12) does not have an analytical solution, but can be solved using numerical methods. The switch voltage for the MOSFET IRF530 is obtained from this equation, as shown in Fig. 2. The values of necessary parameters to solve this equation are shown in Table 2, acquired from the corresponding PSpice models of the IRF510 and IRF530. The ZVS and ZDS conditions can be satisfied in switch voltage. Applying these conditions in (12), results in:
\[
I_{DC} = \frac{I_n \cos(\theta_1 + \varphi) + \cos(\varphi) - k \sin(\varphi) + \omega C_{gd} V_{th}}{\pi - \theta_1 + k}, \tag{14}
\]
while applying the conditions in (6) and (8) result in
\[
I_{DC} + I_n \sin(\varphi) + \frac{\omega C_{gd} V_{th}(\pi)}{k} = 0. \tag{15}
\]
If we assume the high efficiency for the amplifier, the power relations can be written as
\[
P_0 = P_{DC}, \tag{16}
\]
where output power ($P_0$) and DC power ($P_{DC}$) are defined as
\[
P_0 = \frac{R_{in}^2 I_n^2}{2} \tag{17}
\]
and
\[
P_{DC} = V_{DC} \times I_{DC}. \tag{18}
\]
Substituting (17) and (18) in (16), results in
\[
\frac{R_{in}^2}{2} = V_{DC} \times I_{DC}. \tag{19}
\]
Substituting (14) in (19) forms a quadratic equation, which one of the solution is
\[
I_n = \frac{V_{DC} \left( A + \sqrt{A^2 + 2(\omega R_s C_{gd} V_{th}(\pi - \theta_1 + k)/V_{DC})} \right)}{R(\pi - \theta_1 + k)}, \tag{20}
\]
where $A$ is defined as
\[
A = \cos(\varphi) + \cos(\theta_1 + \varphi) - k \sin(\varphi). \tag{21}
\]
The other solution is not acceptable. Then, according to (19), the DC current ($I_{DC}$) will be obtained as
\[
I_{DC} = \frac{V_{DC} \left( A + \sqrt{A^2 + 2(\omega R_s C_{gd} V_{th}(\pi - \theta_1 + k)/V_{DC})} \right)^2}{2R(\pi - \theta_1 + k)^2}. \tag{22}
\]
The DC voltage drop across the dc-feed inductance ($L_{RFDC}$) is zero; therefore the average value of the switch voltage, among a period is equal to $V_{DC}$
\[
V_{DC} = \int_0^{\pi/2} v_{gs}(\theta)d\theta = \frac{\int_0^{\pi/2} v_{gs}(\theta)d\theta}{\pi/2}. \tag{23}
\]
The value of $\varphi$ can be obtained, by substituting (20) and (22) in (15), while satisfying (23). The switching voltage is zero during $\pi \leq \theta < 2\pi$, so the integration can be performed on the first half of the period in (23). Equation (23) does not have a closed form solution and can be solved numerically. The obtained switch voltage with

**Fig. 2** Waveforms of the switch voltage for the designed class E PA using different values of input voltage and input resistance

<table>
<thead>
<tr>
<th>Table 2 Parameters of IRF530 and IRF510 MOSFETs</th>
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<tbody>
<tr>
<td>$V_{th}$</td>
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<tr>
<td>---------</td>
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<tr>
<td>IRF530</td>
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<tr>
<td>IRF510</td>
</tr>
</tbody>
</table>

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different values of input voltage and input resistance, considering 12 V DC supply voltage, is shown in Fig. 2. According to this figure, as these parameters change, the switch voltage moves and also affects the design parameters. As input voltage and input resistance increase, maximum switch voltage and \( \theta_1 \) become larger. The value of \( \theta_1 \) is shown in Fig. 2 for the case with 10 V input voltage and \( R_S \) of 50 \( \Omega \). The higher maximum switch voltage can result in a lower output power capability, so lower values of \( V_{in} \) and \( R_S \) are desired. Fig. 2 also shows the switch voltage of the conventional circuit, which was illustrated in Fig. 1a. Changes in the input voltage do not affect the specifications of the ideal conventional class E circuit with no parasitic elements.

If the \( R_S \) is considered to be zero, then \( C_{gs} \) can be disregarded and (12) can analytically be solved. Then the switch voltage will be obtained as follows [28].

\[
v_s = 2gV_{in}
\]

where, \( g \) and \( h \) are defined in (10) and (11), respectively, assuming \( \theta_1 \) is zero. The voltage waveforms of the circuit elements in the designed class E amplifier are shown in Fig. 3.

The gate-to-source voltage can be divided in three regions. First is \( 0 \leq \theta < \theta_1 \) when the switch voltage is still zero and the MOSFET is on. Second is \( \theta_1 \leq \theta < \pi \) which is described in (9) and the third is \( \pi \leq \theta < 2\pi \). In the first region, switch is in the on-state, so the \( R_S \) along with, \( C_{gs} \) and \( C_{gd} \) form an RC circuit. Therefore, the gate-to-source voltage could be obtained as

\[
v_{gs} = V_{in}e^{-\theta/\theta_1}.
\]

The switch voltage is zero in the first region, hence it causes a delay

---

**Fig. 3** Waveforms of the input voltage \( v_{in} \), gate-to-source voltage \( v_{gs} \), switch voltage \( v_s \), output voltage \( v_o \), voltage across the series resonant circuit \( v_{LC} \), fundamental component of switch voltage \( v_{s1} \) and fundamental component \( v_{Lx1} \) of voltage across the \( L_x \) in the designed class E PA when \( R_S = 10 \Omega, \ V_{DC} = 12 \ V, \ V_{in} = 10 \ V \) and \( f = 1 \ MHz \).

**Fig. 4** Values of \( \varphi \), \( \omega R_C \) and \( \omega X_C \) using different values of \( R_S \) and \( V_{in} \)

\( a \) \( \varphi \) as a function of \( V_{DC} \)

\( b \) \( \omega R_C \) as a function of \( V_{DC} \)

\( c \) \( \omega X_C \) as a function of \( \omega R_C \)
in the switch voltage waveform, as shown in Fig. 2. The second region is \( \theta_1 \leq \theta < \pi \), where \( \theta_1 \) can be obtained from (25) as
\[
\theta_1 = k \ln \left( \frac{V_{in}}{P_{in}} \right). \tag{26}
\]
In the third region, the initial gate-to-source voltage is \( V_{gs}(\pi) \), while the input voltage is equal to \( V_{in} \). Therefore the gate-to-source voltage increases from \( V_{gs}(\pi) \) to \( V_{in} \) and can be calculated as
\[
V_{gs} = \left( V_{gs}(\pi) - V_{in} \right) e^{\left( 2\pi k / a \right)} + V_{in}. \tag{27}
\]
The MOSFET is still off until the gate-to-source voltage in (27) increases to the threshold voltage. As it is shown in Fig. 3, the ideal input square waveform is deformed in the gate by input series resistance and input parasitic capacitances.

The design parameters could be obtained using (12) and (23). The parameters correspond to the switch voltage \( \phi \), \( g \), \( V_{DC} \), \( V_{in} \), \( \omega R C \), \( \omega R C g \) and \( k \). The values of \( \phi \) and \( \omega R C \) against \( V_{DC} \) are shown in Figs. 4a and b. The obtained values satisfy ZVS and ZDS conditions, (12), (15) and (23). As seen in Fig. 4a, \( \phi \) is illustrated as a function of \( V_{DC} \) using different values of \( R_S \) and \( V_{in} \) while the other parameters are constant. According to this figure as \( R_S \) or \( V_{in} \) decreases, \( \phi \) reaches to the constant value of \(-0.567\) rad. However, for all of the different values in Fig. 4a, \( \phi \) increases as the DC voltage increases. If the \( R_S \) is considered to be zero, then the value of \( V_{in} \) does not affect the switch voltage and leads to the constant value of \( \phi \).

Fig. 4b shows \( \omega R C \) as a function of \( V_{DC} \) using different values of \( R_S \) and \( V_{in} \). For each value of \( \omega R C \) the switch voltage \( (v_s) \) and appropriate value of \( \phi \) are obtained using (12) and (15), considering the other parameters are constant. As the DC supply voltage \( (V_{DC}) \) changes, the appropriate value of \( \omega R C \) can be found to satisfy (23). According to the Fig. 4b the value of \( \omega R C \) will be decreased as the DC supply voltage decreases. The inductive reactance of \( L_s \) can be defined as [14],
\[
X = R \tan(\varphi_1 - \varphi). \tag{28}
\]
\( \varphi_1 \) can be defined as follows [14]
\[
\varphi_1 = \tan^{-1} \left( \frac{\int_{\theta_1}^{\pi} v_s(\theta) \cos(\theta)d\theta}{\int_{\theta_1}^{\pi} v_s(\theta) \sin(\theta)d\theta} \right) . \tag{29}
\]
It is seen from (29) that \( \varphi_1 \) is a function of switch voltage and parameters which affect the switch voltage. Fig. 4c shows \( \omega R C \) as a function of \( \omega R C \) using different values of \( R_S \) and \( V_{in} \), while the other parameters are constant. The conventional class \( E \) circuit results are also shown in Fig. 4.

### 3 Power capability

The output power capability, \( C_P \), is generally used to study the output power of a class \( E \) PA. The \( C_P \) is defined as output power, which is produced when the peak switch voltage is equal to 1 V and peak switch current is equal to 1 A. The \( C_P \) equation can be written as
\[
C_P = \frac{P_{o,max}}{V_{s,max} I_{s,max}}, \tag{30}
\]
where, \( P_{o,max} \) is the maximum output power which is equal to the input power \( (V_{DC} \times I_{DC}) \). Moreover, \( V_{s,max} \) is maximum value of switch voltage which appears during the first half period \((0 \leq \theta < \pi)\), while \( I_{s,max} \) is maximum value of switch current which occurs during the second half period \((\pi \leq \theta < 2\pi)\). Equation (30) can be rewritten as
\[
C_P = \frac{1}{(V_{s,max} / V_{DC})(I_{s,max} / I_{DC})}, \tag{31}
\]
where \( I_{s,max} \) is equal to \( I_{s,DC} \). Therefore
\[
\frac{I_{s,max}}{I_{DC}} = 1 + \frac{I_n}{I_{DC}} \quad 1 + \frac{2(\pi - \theta_1 + k)}{A + \sqrt{A^2 + (2\omega R C g V_{DC} \theta(\pi - \theta_1 + k)/V_{DC})}}. \tag{32}
\]

---

Maximum value of switch voltage \(v_{\text{v, max}}\) occurs when derivative of switch voltage \(v_{\text{v}}\) is zero at the \(\theta = \theta_{\text{max}}\). The relation between \(v_{\text{v, max}}\) and \(\theta_{\text{max}}\) can be obtained using (12) as

\[
v_{\text{v, max}} = \frac{2gV_{\text{bi}}}{V_{\text{DC}}} \left( g + H(\theta_{\text{max}}) - \sqrt{g^2 + 2gH(\theta_{\text{max}}) + 1} \right),
\]

where \(H\) is defined as

\[
H(\theta_{\text{max}}) = h(\theta_{\text{max}}) + \frac{k(I_{\text{DC}} - I_{\text{m}} \sin(\theta + \phi))}{2\alpha C_{\text{th}} V_{\text{bi}}}.
\]

As it can be seen from (33), \(v_{\text{v, max}}\) is a function of parameters, which are corresponding to the switch voltage. Fig. 5a shows the \(v_{\text{v, max}}/V_{\text{DC}}\) as a function of \(V_{\text{DC}}\) using different values of \(R_{\text{S}}\) and \(V_{\text{m}}\). According to this figure, increasing in \(R_{\text{S}}\) and \(V_{\text{m}}\) rises the maximum voltage. Fig. 5b shows the \(i_{\text{v, max}}/I_{\text{DC}}\) as a function of \(V_{\text{DC}}\). As seen in this figure, as \(R_{\text{S}}\) or \(V_{\text{m}}\) decreases, the value of \(i_{\text{v, max}}/I_{\text{DC}}\) reaches to the constant value of 2.86, which is shown in Fig. 5b. According to (31)–(33), the output power capability for the class \(E\) PA can be written as (see (35))

Fig. 5c shows the output power capability for the designed class \(E\) PA as a function of \(V_{\text{DC}}\) using different values of \(R_{\text{S}}\) and \(V_{\text{m}}\). According to the figure, it is seen that the output power capability decrease as the \(R_{\text{S}}\) and \(V_{\text{m}}\) increase. From (31) it can be concluded that \(C_{\text{P}}\) is proportional to the inverse of \(v_{\text{v, max}}/V_{\text{DC}}\); hence when maximum of \(v_{\text{v, max}}/V_{\text{DC}}\) occurs, then minimum of the \(C_{\text{P}}\) will be achieved. The change in \(i_{\text{v, max}}/I_{\text{DC}}\) is small for \(V_{\text{DC}}\) of more than 10 V. The \(C_{\text{P}}, v_{\text{v, max}}/V_{\text{DC}}\) and \(i_{\text{v, max}}/I_{\text{DC}}\) are constant versus \(V_{\text{DC}}\) for the conventional circuit, as illustrated in Fig. 5.

4 Gate driver circuit

The gate driver is an important block in class \(E\) PA design, because the MOSFET will not operate as expected if its input is not driven properly. Therefore, the resulting output stage performance might or might not be acceptable [37]. The driver stage specifications should be well chosen to satisfy the desired design parameters. The average power dissipated at the gate port is defined as

\[
P_G = \frac{1}{2\pi} \int_0^{2\pi} R_{\text{th}} \sin^2 \theta \, d\theta,
\]

where \(I_{\text{m}}\) is the input current. The driver equivalent circuit used in this paper is shown in Fig. 6a. According to Fig. 6c more output power capability can be obtained using lower input voltage and input series resistance. As mentioned before, \(R_{\text{S}}\) represents both MOSFET gate resistance and output resistance of the amplifier driver. The MOSFET gate resistance is chosen to be 4.63 Ω according to the PSpice model and the measured output resistance of the amplifier driver is considered. Therefore, the applied circuit provides a 5 V square voltage and 10 Ω of \(R_{\text{S}}\). Fig. 6b shows the fabricated circuit of the designed class \(E\) PA.

5 Maximum operating frequency

At high frequencies, the MOSFET output capacitance \(C_{\text{ds}}\) becomes higher than the external shunt capacitance. The maximum frequency occurs, when intrinsic MOSFET capacitance \(C_{\text{ds}}\) becomes equal to the external shunt capacitance [38]. ZVS and ZDS conditions should be satisfied in class \(E\) amplifier and the upper limit of the operating frequency will occur, when these conditions cannot be further satisfied. In this paper only the intrinsic drain-to-source capacitance, \(C_{\text{ds}}\), is assumed and the external shunt capacitance is not considered. The maximum operating frequency can be determined from \(\omega R_{\text{th}}\) by setting \(f = f_{\text{max}}\) [38]. The effect of DC supply voltage on the maximum operating frequency is shown in Fig. 7. As can be seen from the figure, the maximum operating frequency for the conventional circuit is constant versus DC supply voltage.

6 Power conversion efficiency and power gain

Actually, the existence of parasitic resistance in each component leads to power losses. The value of the drain efficiency can be obtained by calculating the total power loss. In this paper, the parasitic resistances of dc-feed inductance \(R_{\text{LFC}}\), series resonant circuit \(r_{\text{LC}}\), and the MOSFET on-resistance \(r_{\text{DS}}\) are considered. The power conversion efficiency of the amplifier can be written as

\[
\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{Loss}}},
\]

while the output power, \(P_{\text{out}}\), and the total power loss, \(P_{\text{Loss}}\) are given as

\[
P_{\text{out}} = \frac{1}{2} R_{\text{th}}^2
\]

and

\[
P_{\text{Loss}} = P_{\text{LFC}} + P_{\text{DS}} + P_{\text{LC}}.
\]

As seen from (39), \(P_{\text{Loss}}\) is sum of power losses in each parasitic resistance. The value of \(P_{\text{Loss}}\) is a function of parasitic resistances, dc-feed inductance current \(i_{\text{LFC}}\), load current \(i_{\text{L}}\), and switch
current ($i$). According to (17) and (36) the power gain of the amplifier can be expressed as

$$G = 10 \log \left( \frac{P_o}{P_i} \right). \quad (40)$$

### 7 Simulation and experimental results

In this section, a design example is given to describe the design procedure of a class $E$ PA with proposed considerations and assumptions. The design specifications for the presented PA were input voltage $V_{in} = 5\,\text{V}$, DC supply voltage $V_{DC} = 12\,\text{V}$, operating frequency $f = 1\,\text{MHz}$, input series resistance $R_S = 10\,\Omega$ and loaded quality factor $Q^*_L = 10$. According to Figs. 4a and b the values of $\phi$ and $\omega RC_{0}$ were obtained as $-0.58$ and $0.422$, respectively. Therefore, due to the operating frequency and $\omega RC_{0}$, the value of

Theoretical, Simulation, Measured

<table>
<thead>
<tr>
<th>$V_{in}$</th>
<th>$V_{DC}$</th>
<th>$f$</th>
<th>$L$</th>
<th>$C$</th>
<th>$C_{ERC}$</th>
<th>$V_{o,max}$</th>
<th>$P_{out}$</th>
<th>$G$</th>
<th>$\eta$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$5,\text{V}$</td>
<td>$12,\text{V}$</td>
<td>$1,\text{MHz}$</td>
<td>$58.4,\text{mH}$</td>
<td>$310,\text{pF}$</td>
<td>$420,\mu\text{H}$</td>
<td>$48.23,\text{V}$</td>
<td>$1.47,\text{W}$</td>
<td>$17.14$</td>
<td>$95.5%$</td>
</tr>
</tbody>
</table>

### 8 Conclusion

Equations for waveforms of the class $E$ PA assuming MOSFET input and output parasitic capacitances have been solved. The MOSFET parasitic output capacitance ($C_{0}$) is assumed non-linear while the input capacitances ($C_{gs}$ and $C_{gd}$) are considered linear according to the corresponding MOSFET PSPice model. In addition, the effect of the input resistance on the class $E$ PA specifications has been studied. According to assumptions and considerations, several parameters are added to design equations. The results show that these parameters affect the designed class $E$ PA specifications, such as switch voltage, phase shift and output power capability. For instance, increasing of the $R_S$ and $V_{in}$ results in higher maximum switch voltage and lower maximum switch current, while eventually leads to the lower output power capability. A design example is given to describe the design procedure, which was verified from the quantitative agreements among experimental, simulation, and theoretical results.

### 9 References

38 Kazimierczuk, M.K.: ‘RF power amplifier’ (John Wiley & Sons, 2014)