Analysis and Design of Class DE Amplifier with 
Nonlinear Shunt Capacitance

Hiroo Sekiya*, Takayuki Watanabe*, Tadashi Suetsugu† and Marian K. Kazimierczuk‡
*Graduate School of Advanced Integration Science, Chiba Univ., Chiba, 263-8522 JAPAN
Email: sekiya@faculty.chiba-u.jp
† Dept. of Electronics Engineering, Fukuoka Univ., Fukuoka, 814-0180 JAPAN
Email: suetsugu@fukuoka-u.ac.jp
‡ Dept. of Electrical Engineering, Wright State Univ., Dayton, Ohaio, 45435-0001 USA
Email: marian.kazimierczuk@wright.edu

Abstract—This paper presents the analysis and design of class DE amplifier with nonlinear shunt capacitance. In the past, the researchers clarified class DE amplifier with linear shunt capacitance analytically. For higher frequency operation, however, lower shunt capacitance is required for the design. In this case, shunt capacitance has nonlinearity because of output capacitance of MOSFET. Therefore, it is important to clarify the effect of this nonlinearity to the operation of class DE amplifier analytically. In this paper, analytical expressions are derived as waveforms and design equations. From this analysis, it is clarified that the nonlinearities of shunt capacitances affect the waveforms in the dead-time intervals. The validity of our analysis is confirmed by PSpice simulations and experiments.

I. INTRODUCTION

Class DE amplifier [1]–[5] is realized by adding shunt capacitance to class D amplifier and achieving class E zero-voltage switching (ZVS) and zero-derivative switching (ZDS) at the transistor turn-on [6].

Since the class E switching should be satisfied with two conditions simultaneously, it is difficult to determine the elemental values of class DE amplifier. Therefore, several analyses were carried out to design it [1]–[5]. In all analyses, however, it is assumed that shunt capacitances are linear. In the real circuits, the shunt capacitance is realized by the sum of an external capacitance and the MOSFET shunt capacitances. The problem is that the parasitic capacitance is nonlinear, [7]–[14], but the external capacitance is linear. The external capacitance is much higher than the transistor output capacitance for frequencies in the hundred kHz or a few MHz range. Therefore, the all analyses of the class DE amplifier until now have assumed that the shunt capacitances are linear. However, the shunt capacitances are lower and lower as the operating frequency becomes high. Therefore, the parasitic capacitances of MOSFETs are dominant under high frequency operation so their nonlinearities cannot be neglected. For above reason, it is quite important to clarify the effects of the nonlinearities of the shunt capacitances to the operation and design of the class DE amplifier analytically.

This paper presents the analysis and design of the class DE amplifier with nonlinear shunt capacitances. Analytical expressions are derived as waveforms and design equations. From this analysis, it is clarified that the nonlinearities of shunt capacitances affect the waveforms in the dead-time intervals and the ratio of the supply voltage to the built-in potential of the MOSFET body diode is a very important parameter. The parameters of the nonlinear shunt capacitances are determined from the operating frequency, the load resistance, and the ratio of the supply voltage, and the built-in potential. This result means that the operating frequency is restricted by the nonlinearity of the shunt capacitance if the load resistance and the supply voltage are given as design specifications. By carrying out PSpice simulation, it is confirmed that simulated waveforms are similar to the analytical ones quantitatively, which indicates the validity of our analysis.
clarify the effects of the nonlinearities of the shunt capacitances on the operation and design of the class DE amplifier analytically.

Since the power MOSFET contains a p-n junction body diode, the parasitic capacitance $C_{ds}$ can be expressed by

$$C_{ds} = \frac{C_{j0}}{1 + \frac{v_S}{V_{bi}}} m, \quad (3)$$

where $V_{bi}$ is the built-in potential which typically ranges from 0.5 to 0.9 V, $v_S$ is the drain-to-source voltage, $C_{j0}$ is the capacitance at $v_S = 0$, and $m$ is the grading coefficient of the diode junction [7]–[14].

**IV. Analysis of Class DE Amplifier with Nonlinear Shunt Capacitance**

**A. Assumptions**

The analysis in this paper is based on the following assumptions.

a. Both shunt capacitances are only parasitic capacitances of MOSFETs whose nonlinearities are given by (3) for $m = 0.5$.

b. All passive elements except shunt capacitances are linear elements and do not have parasitic resistances.

c. The quality factor of the resonant filter $Q = \omega L_j/R$ is high enough to generate pure sinusoidal output voltage. The current through the $L_f - C_0$ circuit and the load resistance is sinusoidal at the operating frequency.

d. The duty ratios of the two switches are fixed at $D = 0.25$.

e. It is assumed that the switching pattern is the same as that in Fig. 2 and in Table I.

From the above assumptions, the equivalent model of the Class DE amplifier is given as shown in Fig. I(b).

**B. Waveform Equations**

The analysis is performed in the interval $0 \leq \theta < 2\pi$, where, $\theta = \omega t$ represents the angular time. The output current is assumed to be sinusoidal

$$i_{\omega}(\theta) = I_o \sin(\theta + \varphi). \quad (4)$$

**Time Interval: $0 \leq \theta < \pi/2$**

The switch $S_1$ is turned on at $\theta = 0$. In this time interval, the switch $S_1$ is ON and $S_2$ is OFF as shown in Table I. Therefore, the switch voltages are given by

$$v_{S1}(\theta) = 0, \quad v_{S2}(\theta) = V_{DD}. \quad (5)$$

Since they are constant, the currents through the shunt capacitance $C_{S1}$ and $C_{S2}$ are given as

$$i_{CS1}(\theta) = i_{CS2}(\theta) = 0. \quad (6)$$
Because of the bottom switch is open, its current is
\[ i_{S2}(\theta) = 0. \]  
(7)

From (4), (6) and (7), the current through the switch \( S_1 \) is obtained as
\[ i_{S1}(\theta) = -i_o(\theta) = -I_o \sin(\theta + \varphi). \]  
(8)

**Time Interval: \( \pi/2 \leq \theta < \pi \)**

The switch \( S_1 \) is turned off at \( \theta = \pi/2 \). In this time interval, both switches \( S_1 \) and \( S_2 \) are OFF as shown in Table I. Therefore,
\[ i_{S1}(\theta) = i_{S2}(\theta) = 0. \]  
(9)

From KCL, the relationship for the current is
\[ -\omega C_{ds1} \frac{dv_{S1}(\theta)}{d\theta} + \omega C_{ds2} \frac{dv_{S2}(\theta)}{d\theta} = I_o \sin(\theta + \varphi). \]  
(10)

Moreover, when we consider the relation of the switch voltages, namely, \( v_{S1} = V_{DD} - v_{S2}(\theta) \), the following equation is obtained.
\[ \frac{dv_{S2}(\theta)}{d\theta} = \frac{I_o}{\omega(C_{ds1} + C_{ds2})} \sin(\theta + \varphi). \]  
(11)

Since \( v_{S2}(\pi/2) = V_{DD} \), we have
\[ \omega \int_{V_{DD}}^{v_{S2}} \left( \frac{C_{j0}}{1 + \frac{V_{DD} - v_{S2}}{V_{bi}}} + \frac{C_{j0}}{1 + \frac{v_{S2}}{V_{bi}}} \right) dv_{S2} \]  
\[ = \frac{I_o}{2} \int_{\frac{\pi}{2}}^{\frac{\pi}{2}} \sin(\theta + \varphi) d\theta'. \]  
(12)

The voltage \( v_{S2} \) is obtained in the analytical form by performing the integration of (12)
\[ v_{S2}(\theta) = \frac{V_{DD}}{2} \pm \frac{1}{2} \left( V_{DD}^2 - 4V_{bi} \right) \left[-1 - \frac{V_{DD}}{V_{bi}} + \left[1 + \frac{V_{DD}}{V_{bi}} \right]^{2} \right]^{\frac{1}{2}} \]  
\[ - \frac{1}{2} \left( -I_o(\cos(\theta + \varphi) + \sin \varphi) \right) - 1 + \left[1 + \frac{V_{DD}}{V_{bi}} \right]^{2} \]  
(13)

In (13), the sign “±” of the second term in the right-hand side changes at the boundary of \( v_{S2} = V_{DD}/2 \). Namely, “+” is valid in the interval \( \pi/2 \leq \theta < 2\pi/3 \) and “−” is valid in the interval \( 2\pi/3 \leq \theta < \pi \). Now, the class E switching conditions are considered. From (2) and (10), we have
\[ I_o \sin(\pi + \varphi) = 0 \]  
(14)
\[ \varphi = 0, \pi. \]  
(15)

The phase shift of the output current \( \varphi = \pi \) since it means that the amplitude of the output is positive. From (12) and \( v_{S2}(\pi) = 0 \), we get
\[ \cos \varphi = \frac{-4\omega V_{bi}C_{j0}}{I_o} \left( \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \right). \]  
(16)

The amplitude of the output current is given as
\[ I_o = 4\omega C_{j0}V_{bi} \left( \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \right). \]  
(17)

By substituting (17) into (13), the switch voltage \( v_{S2} \) becomes
\[ v_{S2}(\theta) = \frac{V_{DD}}{2} \pm \frac{1}{2} \left( V_{DD}^2 - 4V_{bi} \right) \left[-1 - \frac{V_{DD}}{V_{bi}} \right]^{\frac{1}{2}} \]  
\[ + \left\{ 1 + \frac{V_{DD}}{2V_{bi}} - \frac{1}{2} \left[ -2 \left( 1 - \left[1 + \frac{V_{DD}}{V_{bi}} \right] \cos \theta \right) \right] - 1 + \left[1 + \frac{V_{DD}}{V_{bi}} \right]^{2} \right\}^{\frac{1}{2}}. \]  
(18)

**Time Interval: \( \pi \leq \theta < 3\pi/2 \)**

The switch \( S_2 \) is turned on at \( \theta = \pi \). In this interval, \( S_1 \) is OFF and \( S_2 \) is ON as shown in Table I. Since the switch voltages are constant
\[ v_{S1}(\theta) = V_{DD}, \quad v_{S2}(\theta) = 0, \]  
(19)
the currents through the shunt capacitances \( C_{S1} \) and \( C_{S2} \) are
\[ i_{CS1}(\theta) = i_{CS2}(\theta) = 0. \]  
(20)

Because \( S_1 \) is open, the current through the switch \( S_1 \) is
\[ i_{S1} = 0. \]  
(21)

From (4), (20) and (21), the current through the switch \( S_1 \) is derived as
\[ i_{S1}(\theta) = -i_o(\theta) = I_o \sin \theta. \]  
(22)

**Time Interval: \( 3\pi/2 \leq \theta < 2\pi \)**

The switch \( S_2 \) is turned off at \( \theta = 3\pi/2 \). In this interval, both switches \( S_1 \) and \( S_2 \) are OFF as shown in Table I, namely,
\[ i_{S1}(\theta) = i_{S2}(\theta) = 0. \]  
(23)

From
\[ -\omega C_{ds1} \frac{dv_{S1}(\theta)}{d\theta} + \omega C_{ds2} \frac{dv_{S2}(\theta)}{d\theta} = -I_o \sin \theta \]  
(24)
and \( v_{S2} = V_{DD} - v_{S1}(\theta) \), the differential equation for the switch voltage \( v_{S1} \) is obtained
\[ \frac{dv_{S1}(\theta)}{d\theta} = \frac{I_o}{\omega(C_{ds1} + C_{ds2})} \sin \theta. \]  
(25)

Because \( v_{S1}(3\pi/2) = V_{DD} \), we can write
\[ \omega \int_{V_{DD}}^{v_{S1}} \left( \frac{C_{j0}}{1 + \frac{V_{DD} - v_{S1}}{V_{bi}}} + \frac{C_{j0}}{1 + \frac{v_{S1}}{V_{bi}}} \right) dv_{S1} \]  
\[ = \frac{I_o}{2} \int_{\frac{3\pi}{2}}^{\frac{3\pi}{2}} \sin(\theta) d\theta. \]  
(26)
The normalized switch voltage $v_{S1}/V_{DD}$.

By calculating the integration of (26) and substituting (17), the switch voltage $v_{S1}$ is derived analytically as

$$v_{S1}(\theta) = \frac{V_{DD}}{2} \pm \frac{1}{2} \left( V_{DD}^2 - 4V_{bi}^2 \left[ -1 - \frac{V_{DD}}{V_{bi}} \right] \cos \theta \right.$$  
$$+ \left( 1 + \frac{V_{DD}}{2V_{bi}} \right) \left( 2 \left( 1 - \sqrt{1 + \frac{V_{DD}}{V_{bi}}} \right) \cos \theta \right.$$  
$$- 1 + \frac{V_{DD}}{V_{bi}} \right)^2 \right)^{\frac{1}{2}}. \tag{27}$$

In (27), the sign “±” of the second term in the right-hand side changes at the boundary of $v_{S1} = V_{DD}/2$. Namely, the sign “+” is valid in the interval $3\pi/2 \leq \theta < 5\pi/3$ and “−” is valid in the interval $5\pi/3 \leq \theta < \pi$.

When both side of (18) are divided by $V_{DD}$, the following equation:

$$\frac{v_{S2}(\theta)}{V_{DD}} = \frac{1}{2} \pm \frac{1}{2} \left( 1 - 4V_{bi}^2 \left[ -1 - \frac{V_{DD}}{V_{bi}} \right] \cos \theta \right.$$  
$$+ \left( 1 + \frac{V_{DD}}{2V_{bi}} \right) \left( 2 \left( 1 - \sqrt{1 + \frac{V_{DD}}{V_{bi}}} \right) \cos \theta \right.$$  
$$- 1 + \frac{V_{DD}}{V_{bi}} \right)^2 \right)^{\frac{1}{2}}. \tag{28}$$

is given. The resulting waveform equations indicate that the difference between amplifiers with the nonlinear shunt capacitances and linear ones appear only during the dead time intervals. Figure 3 shows the normalized voltage waveforms for the bottom switch $v_{S1}/V_{DD}$. From this figure, it is found that the slope of the switch voltage increases when $V_{DD}/V_{bi}$ increases. Namely, the maximum currents through the shunt capacitances are larger due to the nonlinearities of the shunt capacitances.

C. Power Relations

The input power is given by

$$P_{in} = V_{DD}I_D. \tag{29}$$

In (29), the dc input current $I_D$ is expressed as the average of the supply current from the dc voltage source $V_{DD}$, which is given by

$$I_D = \frac{1}{2\pi} \int_0^{2\pi} \{i_{S2}(\theta) + i_{CS2}(\theta)\} d\theta$$  
$$= \frac{1}{2\pi} \int_0^{2\pi} I_o \sin \theta d\theta$$  
$$= 2\omega C_{j0} V_{bi} \left( \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \right). \tag{30}$$

The output power $P_o$ is derived from (17) as

$$P_o = \frac{I_o V_o}{2} = \frac{RI_o^2}{2}$$  
$$= 8\omega^2 C_{j0} RV_{bi}^2 \left( \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \right)^2. \tag{31}$$

On the other hand, $P_o$ is also derived from (17) as

$$P_o = \frac{V_o^2}{2R} = \frac{V_{DD}^2}{2R}. \tag{32}$$

If the power losses on the parasitic resistance are neglected and the identical operation is assumed, the drain efficiency achieves 100% conversion. Namely,

$$P_{in} = P_o. \tag{33}$$

From (29) – (31), the following equation is obtained:

$$\omega C_{j0} R = \frac{V_{DD}/V_{bi}}{4\pi \sqrt{1 + \frac{V_{DD}}{V_{bi}} - 1}}. \tag{34}$$

D. Fourier Analysis

The output voltage $v_o(\theta)$ and the voltage across the resonant inductance $v_L(\theta)$ are expressed as

$$v_o(\theta) = V_o(-\sin \theta), \tag{35}$$

$$v_L(\theta) = V_L(-\cos \theta), \tag{36}$$

where the amplitudes $V_o$ and $V_L$ are

$$V_o = RI_o, \tag{37}$$

$$V_L = \omega LI_o. \tag{38}$$
From (37) and (38), we obtain
\[ \frac{V_o}{V_i} = \frac{\omega L}{R}. \]  
(39)

The amplitudes \( V_o \) and \( V_i \) can be calculated from the Fourier integrals
\[
V_o = \frac{1}{\pi} \int_0^{2\pi} v_s(\sin(\theta))d\theta = \frac{V_{DD}}{\pi},
\]  
(40)
\[
V_L = \frac{1}{\pi} \int_0^{2\pi} v_s(\cos(\theta))d\theta = \frac{V_{DD}}{2},
\]  
(41)

Eqs. (40) and (41) show same expressions as those in [1]. From this result, the output voltage is only determined by the ratio of the supply voltage, and the nonlinearity of the shunt capacitance never affect to the relation of supply and output voltage if class E switching conditions are satisfied.

E. Load Network Elements

Finally, we derive the design equations of the load network. From (40), the output power is
\[ P_o = \frac{V_o^2}{2R} = \frac{V_{DD}^2}{2R\pi^2}. \]  
(42)

Moreover, from (29), (30) and 100% drain efficiency, the output power is given as
\[ P_o = P_{in} = \frac{2\omega V_{bi} C_{j0} V_{DD}}{\pi} \left( \sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1 \right). \]  
(43)

By substituting (43) to (42), the load resistance \( R \) is given as
\[ R = \frac{V_{DD}^2}{2\pi^2 P_o} = \frac{V_{DD}/V_{bi}}{4\pi\omega C_{j0}(\sqrt{1 + \frac{V_{DD}}{V_{bi}}} - 1)}. \]  
(44)

From (39), (40) and (41), the inductance \( L \) is given as
\[ L = \frac{\pi R}{2\omega}. \]  
(45)

Because of the definition of the loaded quality factor \( Q \), the inductance \( L_0 \) is given as
\[ L_0 = \frac{QR}{\omega}. \]  
(46)

From (45) and (46), the inductance \( L_f \) is obtained as
\[ L_f = L_0 - L = \frac{R(2Q - \pi)}{2\omega}. \]  
(47)

The identical resonant filter with resonant frequency \( f = 2\pi\omega \) is realized by \( L_f \) and \( C_0 \). From \( \omega = 1/\sqrt{L_f C_0} \) and (47), the resonant capacitance \( C_0 \) is expressed analytically as:
\[ C_0 = \frac{1}{\omega R(Q - \frac{\pi}{2})}. \]  
(48)

VI. Simulation Verification

In this section, the design example is shown for class DE amplifier with nonlinear shunt capacitance. It is assumed that the shunt capacitance are composed of only parasitic capacitance on MOSFETs and it can be varied arbitrarily.

A. Design Example

At first, the design specifications are given as; the operating frequency \( f = 20 \) MHz, the supply voltage \( V_D = 10 \) V, the output power \( P_o = 1 \) W, the built-in potential of MOSFET \( V_{bi} = 0.7 \) V and the loaded quality factor \( Q = 10 \).

From (44), the load resistance \( R \) is calculated \( R = 5.07 \Omega \). The inductance of the resonant circuit \( L_0 \) is given from (46), that is, \( L_0 = 0.404 \mu \) H. The capacitance of the resonant circuit \( C_0 \) is obtained from (48), that is, \( C_0 = 0.186 \) nF. Finally, \( C_{j0} \) in the nonlinear shunt capacitance is derived from (34), namely, \( C_{j0} = 0.613 \) nF.

B. PSpice Simulation

In this paper, the simulations are performed using the circuit simulator PSpice. We use a power MOSFET Spice model Level 3.

Figure 4 shows the waveforms from analysis and simulations. Figures 4 (a) and (b) are the waveforms from analytical waveform equations, simulated waveforms for \( f = 20 \) MHz, respectively. The analytical equations denote that the waveforms of class DE amplifier with nonlinear shunt capacitance independent on the operating frequency. Both waveforms of switch voltage achieve class E switching conditions and the waveforms in Fig. 4 (b) are quite similar to those in Fig. 4 (a). Zero slope of voltage switching can be confirmed since the output current \( i_o \) is zero at the turn on instant. These results indicate the validity of our analysis.

VI. Conclusion

This paper has presented the analysis and design of the class DE amplifier with nonlinear shunt capacitances. Analytical expressions are derived as waveforms and design equations. From this analysis, it is clarified that the nonlinearities of shunt capacitances affect the waveforms in the dead-time intervals and the ratio of the supply voltage to the built-in potential of the MOSFET body diode is a very important parameter. The parameters of the nonlinear shunt capacitances are determined from the operating frequency, the load resistance, and the ratio of the supply voltage, and the built-in potential. This result means that the operating frequency is restricted by the nonlinearity of the shunt capacitance if the load resistance and the supply voltage are given as design specifications. By carrying out PSpice simulation, it is confirmed that simulated waveforms are similar to the analytical ones quantitatively, which indicates the validity of our analysis.

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The angular time (rad)

The switch voltage $v_s \text{ (V)}$

Driving signal $\text{Dr}_1$
dead time

off

The output current $i_o \text{ (A)}$

Driving signal $\text{Dr}_1$

dead time

off

Fig. 4. Example waveforms of class DE amplifier with nonlinear shunt capacitance. (a) Waveforms from analytical equations, (b) Simulated waveforms for $f=20\text{MHz}$.


